

Abstract of the Disclosure

An integrated circuit driver includes an output stage having source drain paths of a PFET and NFET connected in series with each other across DC power supply terminals. A pair of inverters simultaneously responsive to a bilevel signal drive gate electrodes of the PFET and NFET. Each inverter includes a pair of switches and a resistor for connecting opposite polarity voltage sources to a separate capacitor connected in shunt with gate electrodes of the PFET and NFET. The inverters, resistors and capacitors prevent the PFET and NFET from being on simultaneously.